

WHAT IS CLAIMED IS:

- 1 1. A method of fabricating a transistor, the method comprising:  
2 providing a workpiece;  
3 growing a stressed semiconductor layer over the workpiece;  
4 growing a first layer of silicon and carbon over the stressed semiconductor layer;  
5 depositing a gate dielectric material over the layer of silicon and carbon;  
6 depositing a gate material over the gate dielectric material;  
7 patterning the gate material and gate dielectric material to form a gate and a gate  
8 dielectric disposed over the layer of silicon and carbon; and  
9 forming a source region and a drain region in the layer of silicon and carbon and stressed  
10 semiconductor layer, wherein the source region, drain region, gate, and gate dielectric comprise a  
11 transistor.
- 1 2. The method according to Claim 1, wherein growing the layer of silicon and carbon  
2 comprises epitaxially growing a layer of about 90 to 99.5% silicon and about 0.5 to 10 % carbon  
3 having a thickness of about a few tens of Å to about 5 µm.
- 1 3. The method according to Claim 1, wherein growing the stressed semiconductor layer  
2 comprises epitaxially growing a second layer of silicon and carbon, a layer of silicon and  
3 germanium, or a layer of silicon, carbon and germanium, and wherein growing the stressed  
4 semiconductor layer comprises growing a material having a thickness of about 100 Å to about 5  
5 µm.

1 4. The method according to Claim 1, wherein depositing the gate dielectric material  
2 comprises depositing a high k dielectric material or an oxide, and wherein depositing the gate  
3 material comprises depositing a semiconductor material or a metal.

1 5. The method according to Claim 1, further comprising depositing a thin semiconductor  
2 material over the first layer of silicon and carbon, before depositing the gate dielectric material.

1 6. The method according to Claim 5, wherein depositing the thin semiconductor material  
2 comprises depositing about 100 Å or less of Si, Ge, SiGe, a bilayer of Si/SiGe, or a bilayer of  
3 Ge/SiGe.

1 7. The method according to Claim 1, further comprising forming isolation regions in the  
2 workpiece, before or after growing the stressed semiconductor layer over the workpiece and  
3 growing a first layer of silicon and carbon over the workpiece, and further comprising forming  
4 spacers over sidewalls of the gate and gate dielectric.

1 8. The method according to Claim 1, wherein providing the workpiece comprises providing  
2 a silicon-on-insulator (SOI) wafer.

1 9. A method of fabricating a transistor, the method comprising:  
2 providing a workpiece;  
3 growing a first layer of silicon and carbon over the workpiece;  
4 depositing a gate dielectric material over the layer of silicon and carbon, the gate  
5 dielectric comprising a high dielectric constant (k) material;  
6 depositing a gate material over the gate dielectric material, the gate material comprising a  
7 metal;  
8 patterning the gate material and gate dielectric material to form a gate and a gate  
9 dielectric disposed over the layer of silicon and carbon; and  
10 forming a source region and a drain region in at least the layer of silicon and carbon,  
11 wherein the source region, drain region, gate, and gate dielectric comprise a transistor.

1 10. The method according to Claim 9, wherein growing the layer of silicon and carbon  
2 comprises epitaxially growing a layer of about 90 to 99.5% silicon and about 0.5 to 10 % carbon  
3 having a thickness of about a few tens of Å to about 5 µm.

1 11. The method according to Claim 9, further comprising growing a stressed semiconductor  
2 layer over the workpiece, before growing the first layer of silicon and carbon over the workpiece,  
3 wherein forming the source region and the drain region comprises forming the source region and  
4 the drain region in the stressed semiconductor layer.

1 12. The method according to Claim 11, wherein growing the stressed semiconductor layer  
2 comprises epitaxially growing a second layer of silicon and carbon, a layer of silicon and  
3 germanium, or a layer of silicon, carbon and germanium, and wherein growing the stressed  
4 semiconductor layer comprises growing a material having a thickness of about 100 Å to 5 µm.

- 1 13. The method according to Claim 9, further comprising depositing a thin semiconductor  
2 material over the first layer of silicon and carbon, before depositing the gate dielectric material.
- 1 14. The method according to Claim 13, wherein depositing the thin semiconductor material  
2 comprises depositing about 100 Å or less of Si, Ge, SiGe, a bilayer of Si/SiGe, or a bilayer of  
3 Ge/SiGe.
- 1 15. The method according to Claim 9, further comprising forming isolation regions in the  
2 workpiece, before or after growing the stressed semiconductor layer over the workpiece and  
3 growing a first layer of silicon and carbon over the workpiece, and further comprising forming  
4 spacers over sidewalls of the gate and gate dielectric.
- 1 16. The method according to Claim 9, wherein providing the workpiece comprises providing  
2 a silicon-on-insulator (SOI) wafer.

1 17. A transistor, comprising:  
2 a workpiece;  
3 a stressed semiconductor layer disposed over the workpiece;  
4 a first layer of silicon and carbon disposed over the stressed semiconductor layer;  
5 a gate dielectric disposed over the layer of silicon and carbon;  
6 a gate disposed over the gate dielectric; and  
7 a source region and a drain region formed in the layer of silicon and carbon and stressed  
8 semiconductor layer, wherein the source region, drain region, gate, and gate dielectric comprise a  
9 transistor.

1 18. The transistor according to Claim 17, wherein the layer of silicon and carbon comprises  
2 an epitaxially grown layer comprising about 90 to 99.5% silicon and about 0.5 to 10 % carbon  
3 having a thickness of about a few tens of Å to about 5 µm.

1 19. The transistor according to Claim 17, wherein the stressed semiconductor layer comprises  
2 an epitaxially grown second layer of silicon and carbon, a layer of silicon and germanium, or a  
3 layer of silicon, carbon and germanium, and wherein the stressed semiconductor layer comprises  
4 a thickness of about 100 Å to 5 µm.

1 20. The transistor according to Claim 17, wherein the gate dielectric comprises a high k  
2 dielectric material or an oxide, and wherein the gate comprises a semiconductor material or a  
3 metal.

1 21. The transistor according to Claim 17, further comprising a thin semiconductor material  
2 disposed over the first layer of silicon and carbon.

- 1 22. The transistor according to Claim 21, wherein the thin semiconductor material comprises  
2 about 100 Å or less of Si, Ge, SiGe, a bilayer of Si/SiGe, or a bilayer of Ge/SiGe.
- 1 23. The transistor according to Claim 21, further comprising isolation regions disposed in the  
2 workpiece, and further comprising spacers formed over sidewalls of the gate and gate dielectric.
- 1 24. The transistor according to Claim 21, wherein the workpiece comprises a silicon-on-  
2 insulator (SOI) wafer.

1 25. A transistor, comprising:  
2 a workpiece;  
3 a first layer of silicon and carbon disposed over the workpiece;  
4 a gate dielectric disposed over the layer of silicon and carbon, the gate dielectric  
5 comprising a high dielectric constant (k) material;  
6 a gate disposed over the gate dielectric, the gate comprising metal; and  
7 a source region and a drain region formed in at least the layer of silicon and carbon,  
8 wherein the source region, drain region, gate, and gate dielectric comprise a transistor.

1 26. The transistor according to Claim 25, wherein the layer of silicon and carbon comprises  
2 an epitaxially grown layer comprising about 90 to 99.5% silicon and about 0.5 to 10 % carbon  
3 having a thickness of about a few tens of Å to about 5 µm.

1 27. The transistor according to Claim 25, further comprising a stressed semiconductor layer  
2 formed over the workpiece beneath the first layer of silicon and carbon, wherein the source  
3 region and the drain are also formed in the stressed semiconductor layer.

1 28. The transistor according to Claim 27, wherein the stressed semiconductor layer comprises  
2 a second layer of silicon and carbon, a layer of silicon and germanium, or a layer of silicon,  
3 carbon and germanium, and wherein the stressed semiconductor layer comprises a material  
4 having a thickness of about 100 Å to 5 µm.

1 29. The transistor according to Claim 25, further comprising a thin semiconductor material  
2 disposed over the first layer of silicon and carbon, beneath the gate dielectric material.

- 1 30. The transistor according to Claim 29, wherein the thin semiconductor material comprises  
2 about 100 Å or less of Si, Ge, SiGe, a bilayer of Si/SiGe, or a bilayer of Ge/SiGe.
- 1 31. The transistor according to Claim 25, further comprising isolation regions formed in the  
2 workpiece, and further comprising spacers formed over sidewalls of the gate and gate dielectric.
- 1 32. The transistor according to Claim 25, wherein the workpiece comprises a silicon-on-  
2 insulator (SOI) wafer.